Remarks

The present amendment responds to the Official Action dated June 22, 2004. The Official Action rejected claims 2 and 4 under 35 U.S.C. §112, second paragraph, as being indefinite for lack of antecedent basis. Claims 3 and 4 were rejected under 35 U.S.C. §103(a) over Datar et al. U.S. Patent No. 6,625,740 (Datar) in view of Douglas et al. U.S. Patent No. 6,609,193 (Douglas). These grounds of rejection are addressed below.

Claim 1 was allowed over the prior art of record. Claim 2 was indicated to be allowable if amended to overcome the 35 U.S.C. §112, second paragraph rejection above.

Claim 2 has been amended to provide antecedent basis for the element "an array clock", placing claim 2 in order for allowance. Claim 3 has been amended to be more clear and distinct. Claim 4 has been amended to provide antecedent basis for the element "an array clock." New claims 5 and 6 have been added. Support for these new claims can be found, for example, at pages 14 and 15 of the present specification.

Claims 1-6 are presently pending, with claim 1 allowed and claim 2 in order for allowance.

Specification Amendment

During preparation for this amendment, a typographical error was detected in paragraph beginning at page 3, line 4 and is corrected. The paragraph beginning at page 6, line 16 has been amended to update the references to patent applications.

Section 112, Second Paragraph Rejection of Claims 2 and 4

Claims 2 and 4 have been amended by replacing the term "the array clock" with the term "an array clock" to address the lack of antecedent basis rejection.

The Art Rejections

As addressed in greater detail below, Datar and Douglas do not support the Official Action's reading of them and the rejections based thereupon should be reconsidered and withdrawn. Further, the Applicant does not acquiesce in the analysis of Datar and Douglas made by the Official Action and respectfully traverses the Official Action's analysis underlying its rejections.

Claims 3 and 4 were rejected under 35 U.S.C. §103(a) over Datar in view of Douglas. Datar is entitled "Dynamically Activating and Deactivating Selected Circuit Blocks of a Data Processing Integrated Circuit During Execution of Instructions According to Power Code Bits Appended to Selected Instructions." Referring to Figs. 2-4, Datar's system addresses multiple processors disposed in an integrated circuit. Although not labeled with a reference number or specified in Datar's disclosure, the multiple processors appear to directly connect to each other and memory 207 over a communication bus. In Datar's arrangement, software or firmware

which generates 'Sleep' and 'Active' states is stored in memory 207. The firmware looks ahead to determine which circuit blocks are required in the future to execute an upcoming set of instructions and generates the corresponding power control signals to place a particular circuit block in either a 'Sleep' or 'Active' mode when appropriate. Datar, col. 5, line 55 – col. 6, line 32. Datar does not directly address communication between circuit blocks and how an inactive circuit block effects communication between active circuit blocks.

The Official Action admits that Datar does not teach a scalable pipelined array processor. Douglas fails to cure the deficiencies of Datar as a reference. Douglas addresses an algorithm to clock, clear, and, stall a multi-threaded pipelined instruction decoder of a multi-threaded system to maximize performance and minimize power. As defined in Douglas, a thread is one process of a piece of software that can be executed. Douglas, col. 2, lines 59-63. Douglas simply addresses inactivating stages of a pipeline based on instructions associated with a particular thread. Like Datar, Douglas does not teach and does not suggest a scalable pipelined array processor as claimed.

In contrast to Datar and Douglas, presently amended claim 3 addresses a scalable pipelined array processor which is configured as a 2 x 2 or smaller array processor. See present specification, page 15, lines 10-14. In a 2 x 2 or smaller configuration, the present invention may connect each PE through a cluster switch 171 as shown in Fig. 1 in order to allow PEs to communicate with each other. To determine whether to mask off a PE, the S/P bit is examined in each instruction. Referring to Fig. 1 of the present invention, since the cluster switch contains

one level of multiplexers which are fed by each PE, masking off a PE does not effect the communication between non-masked PEs. Claim 3, as presently amended, reads as follows.

> 3. A method for power control in a scalable pipelined array processor comprising:
>
> configuring the scalable pipelined array as a 2 x 2 or smaller array processor, the scalable pipelined array processor having a plurality of processing elements (PEs), the plurality of PEs being connected to a cluster switch;
>
> controlling the execution of instructions in the plurality of PEs and in a sequence processor (SP) by examining an S/P bit of each instruction;
>
> masking off one or more of the plurality of PEs, with the masked off one or more of the plurality of PEs not executing any instructions, while the non-masked off PEs continue to communicate through the cluster switch without being effected by the masked off PEs; and
>
> maintaining all execution units in masked off PEs in an inactive state to conserve power. (emphasis added)

Even if Datar and Douglas are combined as suggested by the Official Action, that combination does not make obvious the combination of elements of claim 3 as presently amended. Datar and Douglas, separately or in combination, do not teach and do not suggest a scalable pipelined array configured in a 2 x 2 or smaller arrangement as presently claimed. Datar and Douglas, separately or in combination, do not teach and do not suggest multiple PEs connected through a cluster switch as presently claimed. Datar and Douglas, separately or in combination, do not teach and do not suggest "masking off one or more of the plurality of PEs, with the masked off one or more of the plurality of PEs not executing any instructions, while the non-masked off PEs continue to communicate through the cluster switch without being effected by the masked off PEs," as presently claimed in claim 3.

The relied upon references fail to recognize and address the problems in the manner advantageously addressed by the present claims. The claims as presently amended are not taught, are not inherent, and are not obvious in light of the art relied upon.

Conclusion

All of the presently pending claims, as amended, appearing to define over the applied references, withdrawal of the present rejection and prompt allowance are requested.

Respectfully submitted,

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